A Novel Dimension-Reduction Technique for the Capacitance Extraction of 3-D VLSI Interconnects

Wei Hong, *Member, IEEE,* Wei-Kai Sun, *Student Member, IEEE,* Zhen-Hai Zhu, Hao Ji, Ben Song, and Wayne Wei-Ming Dai, *Senior Member, IEEE*

***Abstract*—In this paper, a new capacitance extraction method called the dimension-reduction technique (DRT) is presented for three-dimensional (3-D) very large-scale integration (VLSI) interconnects. The DRT converts a complex 3-D problem into a series of cascading simple two-dimensional (2-D) problems. Each 2-D problem is solved separately, thus we can choose the most efficient method according to the arrangement of conductors. We have used the DRT to extract the capacitance matrix of multilayered and multiconductor crossovers, bends, vias with signal lines, and open-end. The results are in close agreement with those of Ansoft's SPICELINK and the Massachusetts Institute of Technolgy's (MIT) FastCap, but the computing time and memory size used by the DRT are several (even ten) times less than those used by SPICELINK and FastCap.**

***Index Terms*— Capacitance extraction, dimension-reduction technique, interconnects, 3-D VLSI.**

I. Introduction

With the continuous increase in the clock rate of the high-speed very large-scale integration (VLSI) system and a decrease in the feature size of the interconnects and packages of VLSI circuit chips, the resultant signal delay, crosstalk, distortion and reflection may degrade the system performance. Analysis of these negative effects has become as important as the circuit design. This has increased the interest in efficient methods for calculating electrical parameters of the interconnects and packages.

Many numerical methods have been applied to extract the electrical parameters of the interconnects and packages. These methods can be generally classified into two categories: integral-equation methods and differential-equation methods. The differential-equation methods, such as the finite-element method (FEM) [1], finite-difference method (FDM) [2], [4], and measured equation of invariance (MEI) [3], [4], divide an interconnect cell into meshes and lead to a large-scale sparse matrix equation. Though the compressed storage technique and some efficient algorithms may be applied, the solving process is still time consuming and requires huge memory. The integral-equation methods, such as the method of moments (MoM) [5], [6], and the boundary-element method (BEM) [7], [8], divide the surfaces of conductors and the interfaces of dielectric layers into meshes and lead to a comparatively smaller, but full matrix. When the numbers of conductors and dielectric layers increase, the analysis procedure will also be too costly in terms of computing time and memory needs.

Until now, several commercial tools such as TMA's Raphael (based on the FDM), Ansoft's SPICELINK (based on the FEM) and the Massachusetts Institute of Technolgy's (MIT) FastCap (based on the multipole accelerated BEM) are available to calculate the capacitance matrix of various interconnects. It is well known that most VLSI interconnects have stratified structures and every layer is homogeneous along the direction perpendicular to the interfaces of the layers (denoted as z-direction). However, it seems that the tools mentioned above have neglected this fact. In this paper, we present a new capacitance extraction method [called the dimension-reduction technique (DRT)] to take full advantage of this fact. According to the method of separation of variables, the three-dimensional (3-D) Laplace equation defined in each layer can be reduced to a two-dimensional (2-D) Helmholtz equation defined on the cross section of the layer because the layer is homogeneous along the z-direction. Therefore, the original 3-D problem is converted into a series of cascading 2-D problems. Each 2-D problem can be solved separately, thus we can choose the most efficient method for each problem according to the arrangement of the conductors. More importantly, it is very easy to obtain the analytical solutions of 2-D problems in many layers such as the pure dielectric layers and the layers with parallel signal lines. Therefore, the domain that has to be analyzed numerically is reduced to the least. This leads to a dramatic reduction in computing time and memory needs. This method has been used to extract the capacitance matrix of multilayered and multiconductor crossovers, bends, via with signal lines, and open-end. The results are in close agreement with those of SPICELINK and FastCap, but the computing time and memory size used by the DRT are several (even ten) times less than those used by SPICELINK and FastCap.

Manuscript received April 19, 1996; revised May 11, 1998. This work was supported by the China National Science Foundation under Grant 69625102.

W. Hong and B. Song are with the State Key Laboratory of Millimeter Waves, Southeast University, Nanjing 210096, China (e-mail: weihong@seu.edu.cn).

W.-K. Sun and Z.-H. Zhu are with Ultima Interconnect Technology Inc., Sunnyvale, CA 94089 USA (e-mail: swka@ultimatech.com).

H. Ji and W. W.-M. Dai are with the Department of Computer Engineering, University of California at Santa Cruz, Santa Cruz, CA 95064 USA (e-mail: dai@cse.ucsc.edu).

Publisher Item Identifier S 0018-9480(98)05518-5.

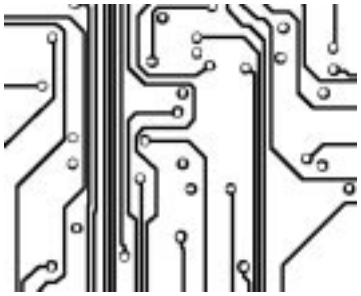


Fig. 1. An example of layout.

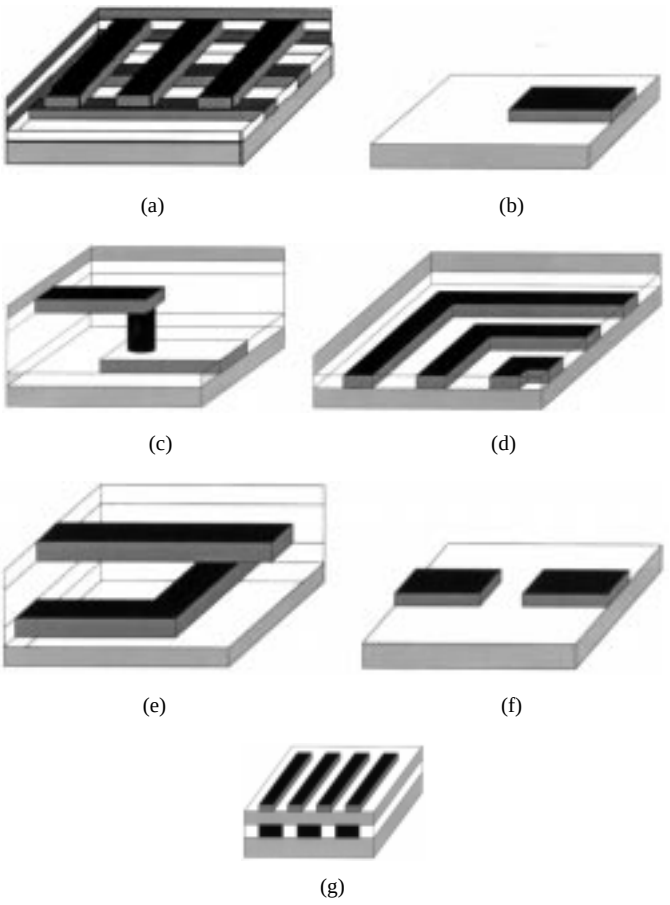


Fig. 2. Some typical interconnect structures. (a) Multiconductor crossover. (b) Open-end. (c) Via with signal lines. (d) Bends. (e) Crossover with bend. (f) Gap. (g) Multilayered multiconductor lines.

II. The Principle of DRT

Up to now, the feature size of VLSI interconnects is far small in comparison with the operation wavelength. Therefore, the static assumption is valid. A simple example of interconnect layout is shown in Fig. 1. To be mentioned later, we assume that the whole interconnect system can be decomposed into a lot of simple cells with magnetic walls and analyzed individually, and these cells can be classified into a limited number of typical structures, such as those shown in Fig. 2.

We will use an example to validate the above decomposing concept. A combined structure in Fig. 3 can be decomposed

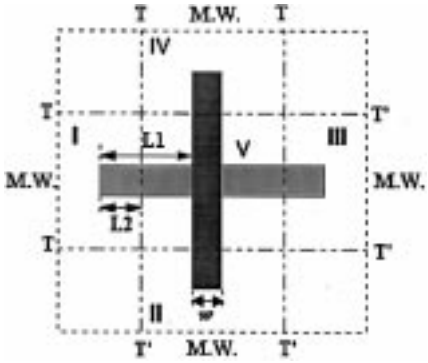


Fig. 3. Crossover with open-end and its decomposition.

TABLE I
Validation of Decomposing Concept ($L1 = 6w$). $C1(1,1) = 2.33 \times 10^{-3}$ pF, $c1(1,2) = -0.298 \times 10^{-3}$ pF

$L2$	$0.5w$	w	$2w$	$3w$	$4w$	$5w$
C_0 (10^{-3} pF)	0.192	0.273	0.430	0.585	0.735	0.741
$C_c(1,1)$ (10^{-3} pF)	1.94	1.80	1.47	1.16	0.835	0.453
$C_c(1,2)$ (10^{-3} pF)	−0.305	−0.304	−0.300	−0.300	−0.281	−0.198
$C2(1,1)$ (10^{-3} pF)	2.324	2.333	2.330	2.330	2.305	1.935
error %	0.25	0.13	0.0	0.0	1.07	16.95
$C2(1,2)$ (10^{-3} pF)	−0.305	−0.304	−0.300	−0.300	−0.281	−0.198
error %	2.35	2.01	0.67	0.67	5.7	33.56

into five cells with magnetic walls; these cells are classified as crossover and open-end. The width and thickness of each conductor are equal and are denoted as w, the length of every conductor is $13w$, the thickness and relative dielectric constant of every dielectric layer are w and 3.9, respectively. First, we compute the capacitance matrix by taking the whole structure as one piece. The matrix is denoted as $[C1]$, and its elements are shown in Table I. Next, we calculate the capacitance of open-end C_0 and the capacitance matrix of crossover $[C_c]$ separately. The capacitance matrix of the whole structure is obtained by the following formula:

$$[C2] = \begin{bmatrix} C_c(1,1) + 2C_0 & C_c(1,2) \\ C_c(2,1) & C_c(2,2) + 2C_0 \end{bmatrix}. \quad (1)$$

The elements of $[C2]$ are shown in Table I, where $L1$ stands for the distance between the edge of the conductor and the end of the open-end, and $L2$ stands for the distance between the magnetic wall and the end of the open-end, as shown in Fig. 3. It is obvious that the error caused by the magnetic walls is less than 5% when $0.5w \leq L2 \leq 4w$.

We will use a typical 3-D multilayer and multiconductor interconnect structure, as shown in Fig. 4, to illustrate the principle of the DRT. Along the interfaces of dielectric layers, the whole structure is cut into slices, as shown in Fig. 4. In the ith slice, the potential function $\phi^{(i)}$ satisfies the 3-D Laplace

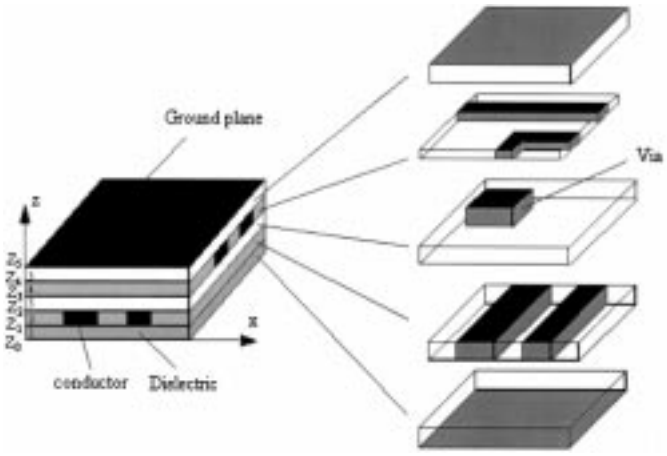


Fig. 4. A 3-D interconnect and slices.

equation

$$\frac{\partial^2\phi^{(i)}}{\partial x^2}+\frac{\partial^2\phi^{(i)}}{\partial y^2}+\frac{\partial^2\phi^{(i)}}{\partial z^2}=0. \tag{2}$$

From Fig. 4, it is obvious that each slice is homogeneous along the z-direction. It should be noted that every slice is surrounded by magnetic walls. Thus, the boundary conditions can be expressed as (3a)–(3d), shown at the bottom of this page, where $V_c^{(j)}$ refers to the voltage on the jth conductor, and $\vec{n}$ is the unit vector normal to the magnetic walls. $\Gamma_c^{(j)}$ refers to the sides of the jth conductor, Γ_M refers to the magnetic walls. The condition (3a) will be absent if the slice is a pure dielectric layer. Denote $W^{(i)}(x, y, V_c^{(j)})$ as a linear function of x, y, and $V_c^{(j)}$, and let

$$\phi^{(i)}=\psi^{(i)}+W^{(i)}(x, y, V_c^{(j)}). \tag{4}$$

If there exists such a function $W^{(i)}(x, y, V_c^{(j)})$ that function $\psi^{(i)}(x, y, z)$ satisfies

$$\psi^{(i)}(x, y, z)=0, \qquad Z_{i-1}\le z\le Z_i,\ (x, y)\in\Gamma_c^{(j)} \tag{5a}$$

$$\frac{\partial\psi^{(i)}(x, y, z)}{\partial n}=0, \qquad Z_{i-1}\le z\le Z_i,\ (x, y)\in\Gamma_M \tag{5b}$$

and Laplace equation (2), then from the method of separation of variables, the general solution of $\psi^{(i)}(x, y, z)$ is

$$\psi^{(i)}(x, y, z)=\sum_{m=1} T_m^{(i)}(x, y)L_m^{(i)}(z) \tag{6}$$

where $T_m^{(i)}(x, y)$ and $L_m^{(i)}(z)$ satisfy the following equations, respectively,

$$\frac{\partial^2 T_m^{(i)}}{\partial x^2}+\frac{\partial^2 T_m^{(i)}}{\partial y^2}+(\alpha_m^{(i)})^2 T_m^{(i)}=0 \tag{7a}$$

$$\begin{cases}\dfrac{\partial T_m^{(i)}}{\partial n}=0, & (x, y)\in\Gamma_M\\ T_m^{(i)}=0, & (x, y)\in\Gamma_c^{(j)}\end{cases} \tag{7b}$$

$$\frac{\partial^2 L_m^{(i)}}{\partial z^2}-(\alpha_m^{(i)})^2 L_m^{(i)}=0. \tag{8}$$

The solution of (7) is called mode functions. The general solution of (8) is

$$L_m^{(i)}(z)=\begin{cases}A_m^{(i)}\cosh(\alpha_m^{(i)}z)+B_m^{(i)}\sinh(\alpha_m^{(i)}z), & \alpha_m^{(i)}\neq 0\\ A_0^{(i)}z+B_0^{(i)}, & \alpha_m^{(i)}=0\end{cases} \tag{9}$$

where $A_m^{(i)}$ and $B_m^{(i)}$ are the undetermined coefficients. Substituting the mode functions, and (4), (6), and (9) into (3c) and (3d), and making the inner product of each side of (3c) with the mode functions, we can obtain a system of linear equations about $A_m^{(i)}$ and $B_m^{(i)}$ by utilizing the orthogonal property of mode functions. The potential functions in every slice and then the capacitance matrix can be readily retrieved from the solutions of these equations.

Therefore, the crux of the whole problem has become how to efficiently solve Helmholtz equation (7). In the pure dielectric layer, such as the first and fifth layer in Fig. 4, the mode functions and eigenvalues have the analytical expressions as

$$T_m^{(i)}(x, y)=\cos\left(\frac{(p-1)\pi x}{a}\right)\cos\left(\frac{(q-1)\pi y}{b}\right) \tag{10a}$$

$$\alpha_m^{(i)}=\pi\sqrt{\left(\frac{p-1}{a}\right)^2+\left(\frac{q-1}{b}\right)^2} \tag{10b}$$

$$p=1, 2, \cdots, NM_x$$
$$q=1, 2, \cdots, NM_y$$
$$m=p+(q-1)NM_x$$
$$i=1, 5$$

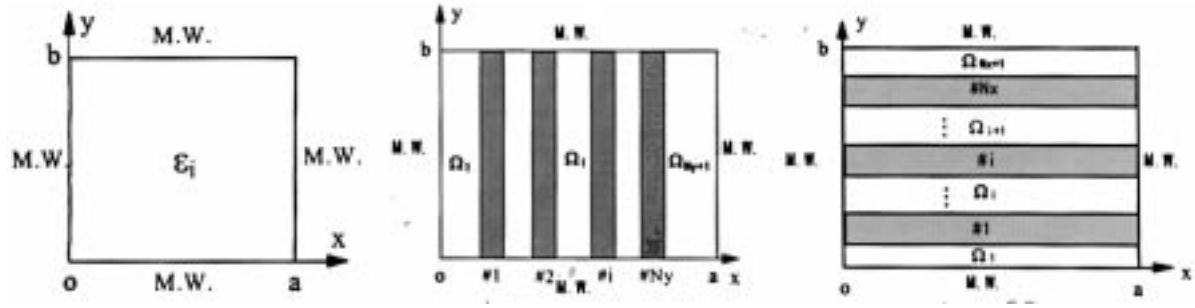
where NM_x and NM_y are the truncated numbers of the mode functions along the x- and y-directions, and a and b are the distance between the magnetic walls along the x-

$$\phi^{(i)}(x, y, z)=V_c^{(j)}, \qquad Z_{i-1}\le z\le Z_i,\ (x, y)\in\Gamma_c^{(j)} \tag{3a}$$

$$\frac{\partial\phi^{(i)}(x, y, z)}{\partial n}=0, \qquad Z_{i-1}\le z\le Z_i,\ (x, y)\in\Gamma_M \tag{3b}$$

$$\begin{cases}\phi^{(i)}=\phi^{(i+1)}\\ \varepsilon_i\dfrac{\partial\phi^{(i)}}{\partial z}=\varepsilon_{i+1}\dfrac{\partial\phi^{(i+1)}}{\partial z}\end{cases}, \qquad z=Z_i \tag{3c}$$

$$\phi^{(1)}(x, y, Z_0)=0$$
$$\phi^{(5)}(x, y, Z_5)=0 \tag{3d}$$



(a) (b) (c)

Fig. 5. Cross section of the typical layers of crossovers in Fig. 2(a). (a) Dielectric layer. (b) y-direction signal-line layer. (c) x-direction signal-line layer.

and y-directions, respectively. For the slice with irregular conductors (such as the fourth layer in Fig. 4), we will choose suitable numerical methods, such as the FDM, to solve (7). The discretized form of (7) can be reduced to the following eigenvalue equation:

$$[S]\overline{T} = \lambda \overline{T} \tag{11}$$

where $\lambda = (\alpha_m^{(i)})^2$ is the eigenvalue, $\overline{T}$ is the eigenvector consisting of the potential value at each mesh node, and $[S]$ is a sparse matrix resulted from the finite-difference (FD) equations at each mesh node. This equation can be solved by some standard subroutines, such as the Lanczos method. And the general solution of potential functions can be expressed as (3). The field matching process is almost the same as that of analytical mode functions.

In summary, the DRT consists of the following four steps:

1) partitioning the complex interconnects into simple cells with magnetic walls;
2) along the interfaces of the dielectric layers, cutting the stratified structure of each cell into slices;
3) finding the function $W^{(i)}(x, y, V_c^{(j)})$ in (4), following the well-known method of separation of the variables, reducing the 3-D Laplace equation (2) into 2-D Helmholtz equation (7) and solving the Helmhotz equation in the cross section of every slice separately;
4) matching the potential of each slice at the interfaces and solving the linear matrix equation about the unknown coefficients.

The field-matching process is the same as that of the mode-matching technique [9], so we will omit the details of this step. The first and the second steps are fixed and can be easily implemented for all kinds of structures, while the third and fourth steps may need some more explanation. In Section III, we will present further details about them.

III. The Application of the DRT

In this section, we will use the DRT to analyze several typical interconnect structures, shown in Fig. 2. Since these structures are surrounded by magnetic walls, we only need to perform the second, third, and fourth steps cited in Section II.

A. Multiconductor Crossover in Multilayered Dielectric Media

The structure of the multiconductor crossover is shown in Fig. 2(a). Based upon the DRT concept, the structure is cut into slices. There are three kinds of slices:

1) pure dielectric layers;
2) layer with y-direction signal lines;
3) layer with x-direction signal lines.

Their cross sections are shown in Fig. 5, where N_x and N_y are the number of the signal lines along x- and y-directions, respectively. The function $W^{(i)}(x, y, V_c^{(j)})$ in (4) can be easily obtained. For the layer with the x-direction signal lines, it is

$$W^{(i)}(y, V_x^{(j)}) = \begin{cases} V_x^{(1)}, & \Omega_1 \\ \dfrac{y - y_{j-1,2}}{SX_j}(V_x^{(j)} - V_x^{(j-1)}) + V_x^{(j-1)}, & \Omega_j \\ V_x^{(N_x)}, & \Omega_{N_x+1} \end{cases} \tag{12}$$

where $V_x^{(j)}$ is the voltage on the jth signal line, SX_j is the distance between jth and $(j-1)$th line. For the layer with y-direction signal lines, $W^{(i)}(x, y, V_c^{(j)})$ takes the similar form.

The mode functions and eigenvalues in every layer can then be expressed analytically; for the pure dielectric layers, they are (10), and for the layer with x-direction signal lines, they are

$$T_m^{(k,i)}(x, y) = \cos\left(\frac{(p-1)\pi x}{a}\right) g_q^{(i)}(y), \qquad i = 1, 2, \cdots, N_x+1 \tag{13a}$$

$$\begin{aligned} p &= 1, 2, \cdots, NM_x \\ q &= 1, 2, \cdots, NM_y^{(i)} \\ m &= p + (q-1)NM_x + \sum_{j=1}^{i-1} NM_x NM_y^{(j)} \end{aligned}$$

$$g_q^{(i)}(y) = \begin{cases} \cos\dfrac{(q-0.5)\pi y}{y_{1,1}}, & i = 1 \\ \sin\dfrac{q\pi(y - y_{i-1,2})}{SX_i}, & 2 \le i \le N_x \\ \cos\dfrac{(q-0.5)\pi(y-b)}{b - y_{N_x,2}}, & i = N_x + 1 \end{cases} \tag{13b}$$

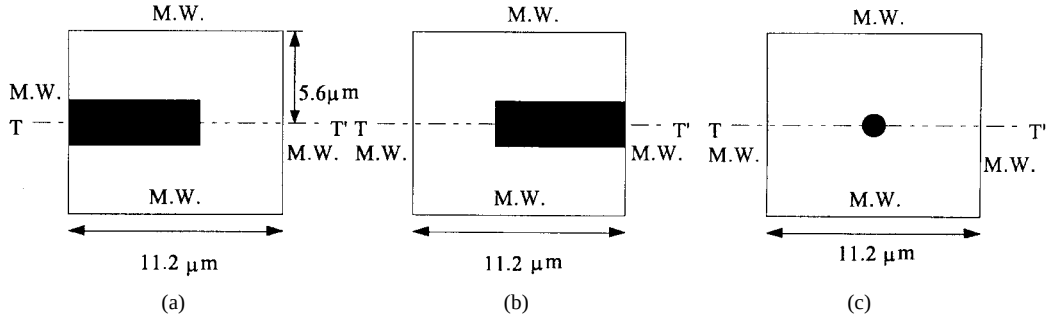


Fig. 6. Cross section of typical layers of the via with signal lines in Fig. 2(c). (a) Top signal line. (b) Bottom signal line. (c) Via.

$$\alpha_m^{(k,i)} = \begin{cases} \pi\sqrt{\left(\dfrac{p-1}{a}\right)^2+\left(\dfrac{q-0.5}{y_{1,1}}\right)^2}, & i=1 \\ \pi\sqrt{\left(\dfrac{p-1}{a}\right)^2+\left(\dfrac{q}{SX_i}\right)^2}, & 2\le i\le N_x \\ \pi\sqrt{\left(\dfrac{p-1}{a}\right)^2+\left(\dfrac{q-0.5}{b-y_{N_x,2}}\right)^2}, & i=N_x+1 \end{cases} \tag{13c}$$

where NM_x and $NM_y^{(i)}$ are the truncated numbers of the mode functions along x- and y-directions in the domain Ω_i, shown in Fig. 5(c), where k is the sequence number of the layer with x-direction signal lines. Exchanging x and y, and a and b, we can obtain the mode functions and eigenvalues in the layer with the y-direction signal lines. Substituting the mode functions of every layer into (6) and matching the potential at the interfaces, we can obtain the capacitance matrix.

The algorithm can be used to analyze crossover with an arbitrary number of lines embedded in an arbitrary number of dielectric layers. The crossover chosen for analysis is modeled as: 1) the number of x- and y-direction lines are two; 2) the width, thickness, and the length of each line are 1, 1, and 8 μm, respectively; 3) the number of dielectric layers is five; 4) the relative dielectric constant and thickness of each layer is 3.9 and 1 μm, respectively; and 5) the crossover is separated from the top and bottom ground planes by 1 μm. The truncated number of mode functions in every layer is 21 $\times$ 21. The capacitance matrix is

$$[C]=\begin{bmatrix} 1.536 & -0.407 & -0.173 & -0.173 \\ -0.407 & 1.535 & -0.173 & -0.173 \\ -0.173 & -0.173 & 1.535 & -0.407 \\ -0.173 & -0.173 & -0.407 & 1.535 \end{bmatrix}\times 10^{-3}\text{pF}. \tag{14}$$

The computing time is 87 s with a SUN SPARC 20 work station and the memory requirement is 2 Mb. We have used Ansoft's SPICELINK to calculate the same structure. The calculated results are

$$[C]=\begin{bmatrix} 1.53 & -0.398 & -0.188 & -0.196 \\ -0.398 & 1.52 & -0.187 & -0.195 \\ -0.188 & -0.187 & 1.47 & -0.373 \\ -0.196 & -0.195 & -0.373 & 1.51 \end{bmatrix}\times 10^{-3}\text{pF} \tag{15}$$

the central processing unit (CPU) time and memory needs are 881 s and 58.551 Mb, respectively.

B. Via with Signal Lines in Multilayered Dielectric Media

The structure of a via with signal lines is shown in Fig. 2(c). The cross sections of three consecutive slices with conductor are shown in Fig. 6.

For these three slices, the function $W^{(i)}(x, y, V_c^{(j)})$ in (4) is

$$W^{(i)}(x, y, V_c^{(j)}) = 1 \tag{16}$$

so the DRT can be applicable to every slice of the whole structure. Since the cross sections in Fig. 6 are irregular, we can only obtain the discrete mode functions of these slices by solving (7) numerically. The mode functions in pure dielectric slices are the same as (10). Substituting all these mode functions into (6) and taking the field-matching step, we can obtain the capacitance. The algorithm can be used for the rectangular via as well as the cases that the signal lines take other shapes (such as a straight line with the pad on top of the via).

We will use the via in Fig. 2(c) as the numerical example. The whole structure can be cut into five slices and is symmetric to the plane $T-T'$, shown in Fig. 6, so we only have to analyze half of the structure. The top and bottom ground planes are separated from the via by 1 μm. The length, width, and thickness of the two signal lines are 6.4, 1.6, and 1 μm, respectively. The radius and height of the via is 0.2 and 3 μm, respectively. The distance between the center of the via and the edge of the signal lines is 0.8 μm. The relative dielectric constant of every layer is 2.5. The capacitance, computing time, and memory size of the DRT and SPICELINK are shown in Table II, where $M1$, $M2$, and $M3$ refer to the truncated number of mode functions in the slices with a top and bottom signal line, the slice with the via, and the pure dielectric slices, respectively.

Since the relative convergence problem is common in the mode-matching method, we have performed a convergence study to see if the DRT will encounter this problem. The curve is shown in Fig. 7, where $M1$ equals $M2$ and the ratio of $M1$ to $M3$ is taken as a variable. From Fig. 7, we can see that the DRT suffers little from the relative convergence problem. Also from Fig. 7, we can see that the result is accurate enough when the mode number in every slice is around 50.

TABLE II
THE CAPACITANCE OF VIA WITH THE SIGNAL LINES

$M1$	$M2$	$M3$	Capacitance in 10^{-3} pF	CPU time in seconds	Memory size in Mb
40	40	49	1.416	85	0.961
50	50	49	1.447	86	0.961
60	60	49	1.430	93	0.961
SpiceLink			1.486	570	54.496

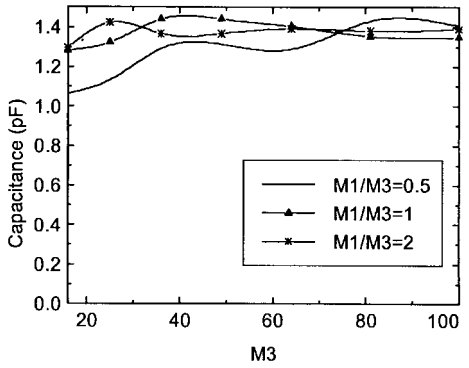


Fig. 7. Convergence study for the structure in Fig. 6.

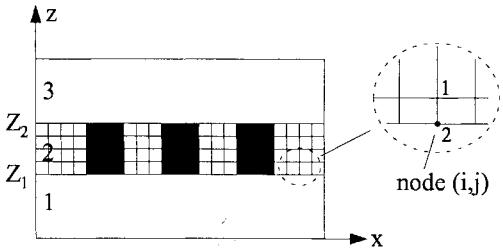


Fig. 8. Side view of the multiconductor bends in Fig. 2(d).

C. Multiconductor Bends in Multilayered Dielectric Media

The multiconductor bends are shown in Fig. 2(d). Unfortunately, for the slice with the conductors, the linear function $W^{(i)}(x, y, V_c^{(j)})$ in (4) does not exist. Therefore, we have to use numerical methods to discretize the Laplace equation (2) in this slice. The side view of the bends with the FD mesh nodes is shown in Fig. 8. The discretized equation (2) can be written as

$$[S]\begin{bmatrix}\overline{\phi}_t\\ \overline{\phi}_{in}\\ \overline{\phi}_b\end{bmatrix} = \overline{V} \tag{17}$$

where vector $\overline{\phi}_t$ and $\overline{\phi}_b$ consists of the potential values at the nodes on the top and bottom interfaces of the slice with bends, $\overline{\phi}_{in}$ consists of the potential values at the nodes between the top and bottom interfaces, and $\overline{V}$ refers to the voltage at the nodes on the surfaces of the bends.

The general solutions in the pure dielectric slice are shown in (6), where the mode functions are still (10). The field-matching process for the bends is different from the standard mode-matching technique. On the interface at $z = Z_1$ (shown in Fig. 8), the first equation in (3c) can be written as

$$\sum_m [A_m^{(i)} \cosh(\alpha_m^{(1)} Z_1) + B_m^{(1)} \sinh(\alpha_m^{(1)} Z_1)] T_m^{(1)}(x, y) = \begin{cases} V^{(k)}, & \text{on the } k\text{th conductor} \\ \overline{\phi}_d(i, j), & \text{otherwise} \end{cases} \tag{18}$$

where (i, j) refers to the mesh number of the node on the dielectric interface. Taking the inner product of both sides of (18) with the mode functions in the pure dielectric slice, we obtain

$$\sum_m [A_m^{(1)} \cosh(\alpha_m^{(1)} Z_1) + B_m^{(1)} \sinh(\alpha_m^{(1)} Z_1)] \cdot \langle T_m^{(1)}(x, y), T_n^{(1)}(x, y)\rangle = \langle V^{(k)}, T_n^{(1)}(x, y)\rangle + \sum_{i=1} \sum_{j=1} \overline{\phi}_d(i, j) T_n^{(1)}(x_i, y_j) \Delta S_{ij}, \quad n = 1, 2, \cdots \tag{19}$$

where (x_i, y_j) refers to the position of the mesh node (i, j) and ΔS_{ij} is the area surrounding the mesh node (i, j). Equation (19) is a linear matrix equation about $A_m^{(i)}$, $B_m^{(i)}$, and $\overline{\phi}_d$. To obtain unique solutions, we have to use the second equation in (3c). However, the mode functions in the slice with bends are unknown, and we cannot take the inner product of both sides with these unknown mode functions. Therefore, we will use the "point-matching technique" instead. The second equation in (3c) is valid only on the discrete mesh nodes. Replacing the differential along the z-direction in the slice with the bends with difference, the second equation in (3c) for the node (i, j) at the dielectric interface is expressed as

$$\epsilon_2 \frac{\phi_1 - \phi_2}{h_z} = \epsilon_1 \frac{\partial}{\partial z} \phi^{(1)}(x_i, y_j, z = Z_1) \tag{20}$$

where ϕ_1 and ϕ_2 are the potential values at node 1 and 2, shown in dashed-line circle of Fig. 8, and h_z is the discretizing step along the z-direction. Combining (19) and (20), we can obtain a matrix equation about $A_m^{(1)}$, $B_m^{(1)}$, and $\overline{\phi}_{in}$, $\overline{\phi}_b$. Similarly, for the interface $z = Z_2$, we can obtain a matrix equation about $A_m^{(3)}$, $B_m^{(3)}$, and $\overline{\phi}_t$, $\overline{\phi}_{in}$. Solving these two matrix equations simultaneously, we can obtain the potential in each slice, and the capacitance matrix can also be readily retrieved.

The multiconductor bends to be analyzed here is modeled as: 1) the number of bends is three; 2) the bends are supported by a layer of dielectric substrate above the bottom ground plane; 3) the thickness and relative dielectric constant of the dielectric layer are 2 μm and 3.9, respectively, and the bends are separated from the top ground plane by a dielectric layer whose thickness and relative dielectric constant are 2 μm and 2.45; 4) the thickness and width of the conductors are 1 and 1.5 μm, respectively; 5) the distance between the conductor is 1.5 μm; and 6) the distance between the magnetic walls along the x- and y-directions are 27 μm. Computed results are

$$[C] = \begin{bmatrix} 1.140 & -0.303 & -0.00616 \\ -0.303 & 1.870 & -0.441 \\ -0.00616 & -0.441 & 2.500 \end{bmatrix} \times 10^{-3}\text{pF}. \tag{21}$$

The computing time is 212 s with the SUN SPARC 20 workstation and memory requirement is 5.8 Mb. The number of mode functions in the dielectric layers is 25×25. We have used the software Ansoft MAXWELL SPICELINK to calculate the same structure, and the computed results are

$$[C] = \begin{bmatrix} 1.140 & -0.304 & -0.00223 \\ -0.304 & 1.990 & -0.461 \\ -0.00223 & -0.461 & 2.580 \end{bmatrix} \times 10^{-3}\text{pF}. \quad (22)$$

The computing time and memory used by SpiceLink are 1541 s and 60.9 Mb.

D. Other Structures

The implementation of the DRT for other structures is straightforward. For instance, to analyze the structure shown in Fig. 2(e), we can use a similar procedure to that used for analyzing the structure in Fig. 2(d). In the layer with a straight line, the mode functions have the similar analytical expressions as (13a), while in the layer with the bend, the mode functions can be obtained numerically. Therefore, combination of the analysis process used for the structures in Fig. 2(a)–(d) can be used to analyze the structure shown in Fig. 2(e)–(g) and almost all kinds of other stratified structures.

IV. Conclusions and Discussion

In this paper, we present a new method named the DRT to extract the capacitance matrix of the 3-D interconnects in VLSI circuits. The method has the following attractive features.

1) The computing time and memory needs are unrelated to the ratio between the thickness of dielectric layers, which means we need not make additional efforts for an interconnect with both very thin and very thick layers. However, it will be very costly to use the FDM and FEM to extract the capacitance matrix of this kind of interconnects.
2) Since the 2-D problems in some layers can be solved analytically, the computing time and memory needs only increase slightly when the sizes of conductors increase. However, the computing time and memory used by the BEM will increase greatly if the same thing happens.
3) The tedious task of a 3-D mesh generation is avoided, since only a 2-D mesh generation is necessary if the 2-D problems in some layers have to be solved numerically.

Based upon the basic idea of the DRT, we can set up an accurate and fast field-solver library for the typical interconnect structures. By using this library, accurate closed-form formulas or database of the electrical parameter of these typical interconnect structures can be easily obtained.

The most fundamental limitation in this approach is that the method of separation of variables is applicable. This requires that the interfaces of each layer are parallel to each other and the surfaces of conductors are either parallel or perpendicular to those interfaces. Unfortunately, some kinds of packages and bonds do not meet these requirements. For these structures, we could use the strategy in Section III-C, i.e., using the 3-D FDM or FEM to analyze the slices containing those "irregular" conductors. In fact, the core concept of the DRT is that every slice is treated separately. Taking the DRT as an algorithm framework, we can develop many hybrid algorithms.

References

[1] T. Chou and Z. J. Cendes, "Capacitance calculation of IC packages using the finite element method and planes of symmetry," *IEEE Trans. Computer-Aided Design,* vol. 13, pp. 1159–1166, Sept. 1994.

[2] M. Naghed and I. Wolff, "Equivalent capacitances of coplanar waveguide discontinuities and interdigitated capacitors using a 3-D finite difference method," *IEEE Trans. Microwave Theory Tech.,* vol. 38, pp. 1808–1815, Dec. 1990.

[3] W. Hong, W. K. Sun, and W. W. M. Dai, "Fast parameter extraction of general three-dimension interconnects using geometry independent measured equation of invariance," presented at the IEEE DAC-96, Santa Cruz, CA, 1996.

[4] W. K. Sun, W. W. M. Dai, and W. Hong, "Fast parameter extraction of general three-dimension interconnects using geometry independent measured equation of invariance," presented at the IEEE DAC-96, Santa Cruz, CA, 1996.

[5] C. Wei, R. F. Harrington, *et al.,* "Multiconductor transmission lines in multilayered dielectric media," *IEEE Trans. Microwave Theory Tech.,* vol. MTT-32, pp. 439–449, Apr. 1984.

[6] K. S. Oh, D. Kuznetsov, and J. E. Schutt-Aine, "Capacitance computations in a multilayered dielectric medium using closed-form spatial green's functions," *IEEE Trans. Microwave Theory Tech.,* vol. 42, pp. 1443–1453, Aug. 1994.

[7] R. Wu, "Resistance computations for multilayer packaging structures by applying the boundary element method," *IEEE Trans. Comp., Packag., Manufact. Technol. C,* vol. 15, Jan. 1992.

[8] K. Nabors and J. White, "Multipole-accelated capacitance extraction algorithms for 3-D structures with multiple dielectrics," *IEEE Trans. Circuits Syst.,* vol. 39, pp. 946–954, Nov. 1992.

[9] Y. C. Shih, "The mode match method," in *Numerical Techniques for Microwave and Millimeter Wave Passive Structures,* T. Itoh, Ed. New York: Wiley, 1989, pp. 592–622.

[10] T. Sakurai and K. Tamaru, "Simple formulas for 2-D and 3-D capacitances," *IEEE Trans. Electron Devices,* vol. ED-30, pp. 183–185, Feb. 1983.

Wei Hong (M'92) was born in Hebei Province, China, in 1962. He received the B.S. degree from the Zhenzhou Institute of Technology, Zhenzhou, China, in 1982, and the M.S. and Ph.D. degrees from Southeast University, Nanjing, China, in 1985 and 1988, respectively, all in radio engineering.

Since 1988, he has been with the State Key Laboratory of Millimeter Waves, Southeast University, where he is currently a Professor and Associate Dean of the Department of Radio Engineering. In 1993, 1995, 1996, and 1997, he was a short-term Visiting Scholar with the University of California at Berkeley and Santa Cruz. He has been engaged in numerical methods for electromagnetic problems, millimeter-wave theory and technology, antennas, electromagnetic scattering, inverse scattering and propagation, RF front-end for mobile communications, and the parameters extraction of interconnects in VLSI circuits, etc. He has authored or co-authored over 150 technical publications and authored *Principle and Application of the Method of Lines* (Nanjing, China: Southeast Univ. Press, 1993). He has also served as a reviewer for *Electronics Letters* and the *Proceedings of the Institution of Electrical Engineers* (IEE), U.K.

Prof. Hong is a senior member of CIE. He was the recipient of the 1992 and 1994 first-class Science and Technology Progress Prizes given by the State Education Commission, the 1991 fourth-class National Natural Science Prize, and the 1988 third-class Science and Technology Progress Prize of Jiangsu Province. He was also the recipient of the Trans-Century Training Programme Foundation for the Talents Award given by the State Education Commission, the Foundation for China Distinguished Young Investigators Award given by the China NSF, the Distinguished China Doctorate Recipients Award given by the State Education Commission, and the JiangSu Young Scientist Award given by the JiangSu Province Government. He has served as the reviewer for many technical journals, including the IEEE Transactions on Microwave Theory and Techniques, IEEE Transactions on Antennas and Propagations, IEEE Transactions on Components, Hybrids, and Manufacturing Technology, and IEEE Transactions on Components, Packaging, and Manufacturing Technology.

Wei-Kai Sun (S'95) was born in Nanjing, China, in 1969. He received the B.Sc. and the M.Sc. degrees from Southeast University (formerly Nanjing Institute of Technology), Nanjing, China, in 1991 and 1994, respectively, both in electrical engineering, and the Ph.D. degree from the University of California at Santa Cruz in 1997.

From 1994 to 1997, he was a Research Assistant at the University of California at Santa Cruz. He is currently with Ultima Interconnect Technology, Inc., Sunnyvale, CA. He has authored or co-authored ten papers in international journals and conference proceedings. His research interests include analytical and numerical methods in computational electromagnetics, circuit and electromagnetic modeling of high-speed and high-frequency interconnections and packages in VLSI and microwave circuits, electromagnetic compatibility (EMC) and electromagnetic interference (EMI), electromagnetic scattering and inverse scattering, and network theory.

Zhen-Hai Zhu was born in Changsha, China, on October 22, 1970. He received the B.S. and Ph.D. degrees in electric engineering from Southeast University, Nanjing, China, in 1992, and 1997, respectively.

From 1992 to 1993, he was a Research Assistant studying scattering and radiation of electric large bodies. From 1994 to 1997, his work was mainly focused on modeling and simulation of 3-D VLSI interconnects embedded in multilayered medium. He has authored and co-authored over ten papers appearing in international journals and conference proceedings. He is currently a Senior Software Engineer at Ultima Interconnect Technology, Inc., Sunnyvale, CA.

Hao Ji was born in Nanjing, China, in 1973. She received the B.S. and M.S. degrees in electrical engineering from Southeast University, Nanjing, China, in 1994 and 1997, respectively, and is currently working toward the Ph.D. degree at the University of California at Santa Cruz.

Her current research interests include computational electromagnetic field and parameter extraction of interconnects in VLSI's and multichip modules (MCM's).

Ben Song was born in Jiangsu Province, China, in 1973. He received the B.S. degree from Nanjing University of Science and Technology, Nanjing, China, in 1994, the M.S. degree from Southeast University, Nanjing, China, in 1997, all in radio engineering, and is currently working toward the Ph.D. degree.

His current research interests includes computational electromagnetic field and parameter extraction of interconnects in VLSI and MCM.

Wayne Wei-Ming Dai (SM'96) received the B.A. degree in computer science and the Ph.D. degree in electrical engineering from the University of California at Berkeley, in 1983 and 1988, respectively.

He is currently an Associate Professor in computer engineering at the University of California at Santa Cruz.

Dr. Dai was an associate editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS and an associate editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE (VLSI) INTEGRATION SYTEMS. He was the founding chairman of the IEEE Multi-Chip Module Conference, which is held annually in Santa Cruz, CA, since 1991. He was the recipient of the 1990 Presidential Young Investigator Award.